Fully Integrated W-CDMA IF Chip-Set for UMTS Mobiles

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Abstract **A fully integrated Silicon-bipolar IF-receiver and IF-transmitter with on-chip synthesizer for use in third-generation variable duplex W-CDMA mobiles is introduced. Both devices incorporate an IF-synthesizer with on-chip VCO tuning and tank as well as 5th order baseband filters and comply with ARIB W-CDMA and UMTS standards. The devices are mounted in a small outline, 32 pin, leadless surface mount package.**

I. Introduction

Third-generation cellular systems, called Universal Mobile Telecommunication System (UMTS), Universal Wireless Communications (UWC-136), Code Division Multiple Access 2000 (cdma 2000), are about to emerge on the market. In Japan UMTS service will be launched in the first quarter of 2001 and in Europe in 2002. In both countries, the Wide-Band Code Division Multiple Access (W-CDMA) scheme will be implemented and enables high data rate applications and services.

This paper describes a fully integrated Si-bipolar low-bias IF-receiver and IF-transmitter for use in third-generation variable duplex W-CDMA mobiles. Either device incorporates an on-chip IF-synthesizer with on-chip VCO tuning and tank as well as 5th-order baseband filters. Both devices comply with ARIB W-CDMA and UMTS standards. The IF-chips are fabricated with Infineons high frequency $0.4\,\mu$m/25 GHz Silicon bipolar process. IF-receiver and IF-transmitter die size is $2.33 \times 2.9\,\text{mm}^2$. Both chips are mounted in a $4.5 \times 5.5\,\text{mm}^2$, 32 pin leadless SMD package of 0.5 mm pitch. The devices are designed for low external component count. The high integration level, together with the small package size, minimizes the required board space of a complete IF-transceiver. The chips operate on 2.7-3.3 V supply, at an ambient temperature range of -30 to +85° and incorporate several power down modes for efficient use in W-CDMA mobile stations.

An overview diagram of the IF-receiver and IF-transmitter is shown in Fig. 1 and Fig. 4, respectively. The W-CDMA IF-receiver includes two complete IF paths for antenna diversity or service channel monitoring. A common LO generation and its distribution via emitter followers drive the two channels. Each path features a variable gain amplifier with > 95 dB gain range at an IF frequency of 318 MHz, a quadrature demodulator and a 5th-order active Chebyshev and a 1st-order allpass anti-aliasing and channel filter[2] with differential I/Q outputs. The IF-synthesizer includes a completely integrated on-chip VCO with integrated transformer and varactor diodes, tuning circuitry and on-chip voltage regulator for the VCO and VCO buffer. A fixed PLL with reference divider, RF prescaler, lock detect circuitry and two on-chip elements of a 3rd-order loop filter complete the on-chip synthesizer. Only three external components are necessary to complete the entire loop filter.

The W-CDMA IF-transmitter features a 5th-order active Butterworth baseband reconstruction-filter[2], that is used for adjacent channel leakage ration minimization as well. It further consists of a quadrature modulator, a variable gain amplifier with > 65 dB gain range at a fixed IF-frequency of 285 MHz. The transmitter IF-synthesizer has the same architecture as the receiver IF-synthesizer, however, does not require a lock detect circuit.
A front-end receiver [4] [5] and front-end transmitter is necessary to complement the presented IF-devices to implement a complete heterodyne transceiver.

Fig. 2 shows the layout of the IF-receiver chip. The synthesizer is located on the right hand half of the chip. The LO divider, the reference divider, the phase comparator and the charge pump are located in the lower right corner, the on-chip VCO, voltage regulator and biasing in the upper right corner, respectively. VCO buffer, the LO divider and some biasing are located just to the left the VCO. On the left hand side two identical receiver paths are placed in parallel. The block visible in the left hand corner is the IF variable gain amplifier, the block below the center is the demodulator and the block above the center the I/Q baseband filters. Fig. 5 shows the layout of the IF-transmitter chip. The synthesizer block is basically the mirror image as compared to the receiver synthesizer. This enables the placement of the devices with an efficient use of board space. The block located in the lower left corner consists of the transmit baseband filters and the block in the upper left corner is the I/Q modulator and the IF variable gain amplifier, respectively. The remaining three circuit blocks are comprised of test circuits.

II. IF-Synthesizer

The fully integrated VCO of the receiver operates at a frequency of 1272 MHz. The fully differential VCO core is in-

ductively coupled via differential 1:1 transformers. This type of VCO has been described in detail by M. Zannoth[3]. An on-chip low voltage drop (350 mV) regulator supplies VCO and VCO buffer and assures 45 dB of power supply rejection up to 1 MHz. Thus, the regulator decouples the external power supply and prevents on-chip crosstalk on supply lines from disturbing the on-chip oscillator. A bandgap reference with a noise floor of -162 dBc/Hz at a supply current of 900 μA and an external reference resistor yield a temperature stable and process independent bias voltage and bias current, respectively. AC-coupling of the oscillator prevents accumulation of dc offsets along the LO chain. Either chip can operate on an external single-ended or differential LO input signal for system flexibility.

III. IF-Receiver

In the receiver section, a divider by two assures a signal of 50 $\pm$1 % duty cycle to the following 0°/90° I/Q master-slave divider. This scheme yields accurate quadratur signals for the Gilbert type mixers of the demodulator, thus, increasing carrier and single-sideband suppression. A three stage variable gain amplifier (VGA) with an input impedance of 1 kΩ// 0.6 pF and a dynamic range of $>$ 95 dB, an input IIP3 of -2 dBm, and a noise figure of 6.5 dB is implemented. The linear-in-dB gain of the VGA is set by an external analog voltage in the range of 0.1 V to 1.75 V. Following the demodulator, 5th-order Chebyschev and 1st-order allpass anti-aliasing filters with I/Q differential outputs are implemented. The filters are composed of 200 MHz to 350 MHz gain-bandwidth product differential operational amplifiers with on-chip RC-networks. The baseband filter is optimized for low amplitude distortion and a linear phase over frequency with $\pm$ 0.5 dB amplitude ripple and $\pm$2° of phase deviation, respectively.

IV. IF-Transmitter

The transmitter path incorporates a 5th-order Butterworth pre-filter for I/Q differential inputs. As in the receiver device, the filters are composed of 200 MHz to 350 MHz gain-bandwidth product differential OpAmps with on-chip RC-networks to minimize pin count and external element count. The baseband filter is optimized for low amplitude distortion and phase distortion and functions as an anti-aliasing filter without degrading error vector magnitude and out-of-band noise performance of the transmitter path. In addition the high open-loop gain of the OpAmps symmetrize the differential input signals considerably, allowing a large range of DC input voltage and even single ended operation. In the transmitter section, again, a divider by two assures a signal of 50 $\pm$1 % duty cycle to the following 0°/90°-I/Q master-slave divider.

A three stage variable gain amplifier (VGA) with open collector output impedance of 20 kΩ//1.0 pF and a dynamic range of $>$ 67 dB, an output noise floor of -129 dBc/Hz at high gain, and an adjacent channel leakage ratio of -53 dBc is implemented. The linear-in-dB gain of the VGA is set by an external analog voltage in the range of 0.1 V to 1.75 V.

V. Measurement Results

A detailed summary of the measured parameters of the presented devices is given in Tab. I. In Fig. 3 the measurement results on the tuning range of the integrated VCO is shown. The tuning characteristic is quite linear. In this case the process was nearly centered, as indicated by the line of nominal VCO frequency 1272 MHz. The diagram also shows the variation of frequency with temperature. The remaining tuning range is utilized to compensate for all process variations. Fig. 6 shows the measurement result of the receiver gain and transmitter gain over gain control voltage.

VI. Conclusion

A complete transceiver chip set consisting of an IF-receiver and IF-transmitter device for use in UMTS mobiles has been presented. The chip set features an on-chip synthesizer and baseband filter in a small outline package, yielding low external chip count, and thus, minimizes required board space. Measurement results emphasize sufficient RF-performance at low bias consumption, and thus, the applicability of the introduced chip set in a W-CDMA mobile station. Both chips are designed to comply with ARIB W-CDMA and UMTS standards.

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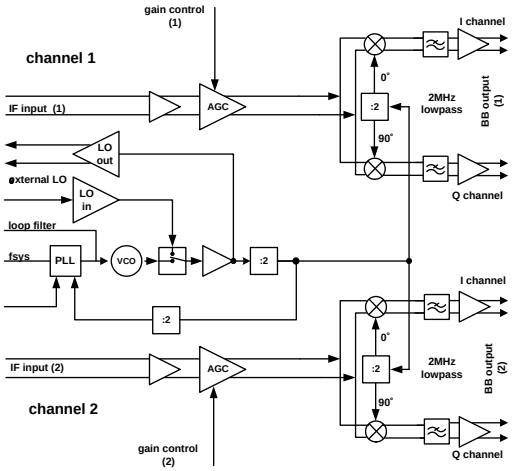

Fig. 1. IF-receiver overview diagram.

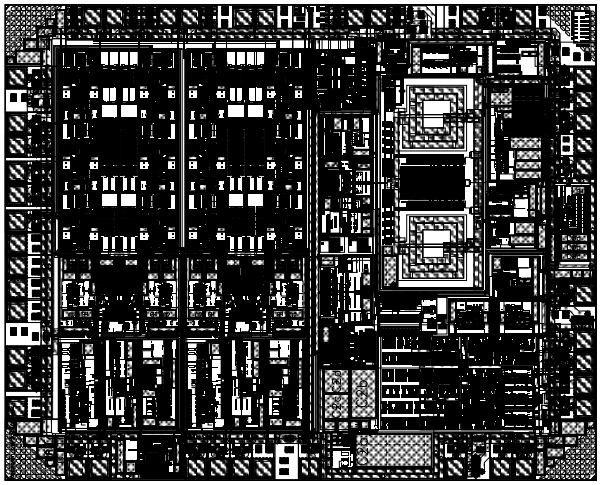

Fig. 2. IF-receiver layout.

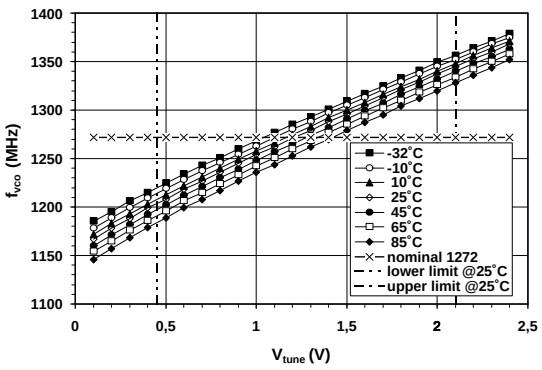

Fig. 3. Measurement of VCO tuning range vs. tuning voltage for a typical process; temperature as parameter.

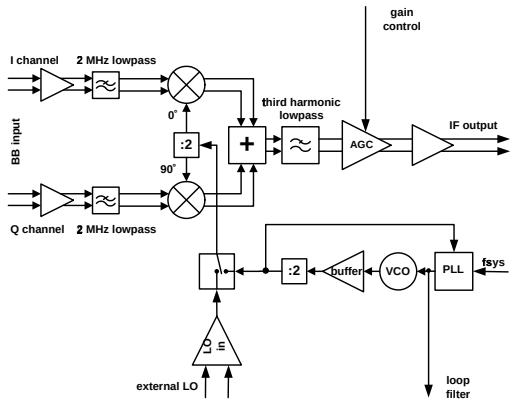

Fig. 4. IF-transmitter overview diagram.

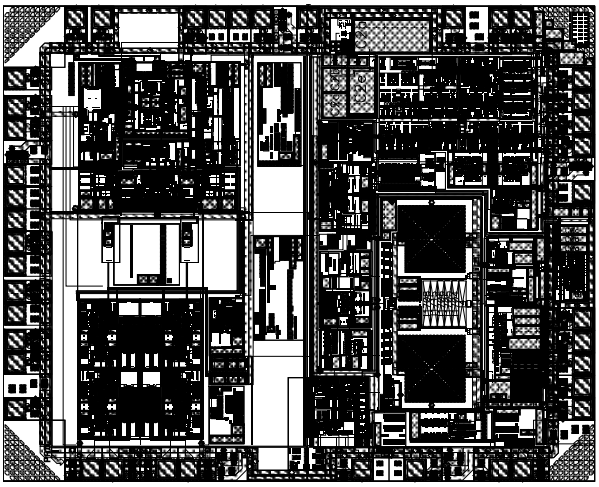

Fig. 5. IF-transmitter layout.

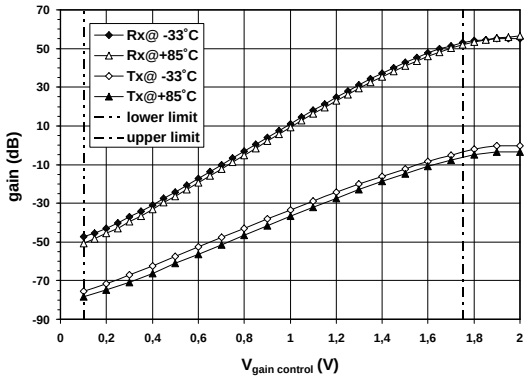

Fig. 6. Measurement of IF-receiver and IF-transmitter gain over gain control voltage.

TABLE I

IF-RECEIVER AND IF-TRANSMITTER INPUT PARAMETERS AND CORRESPONDING MEASUREMENT RESULTS.

function	description	parameter	receiver	transmitter
VCO	frequency	f_{VCO}	1272 MHz	1140 MHz
	tuning sensitivity	k_{VCO}	75 MHz/V	75 MHz/V
IF	frequency	f_{IF}	100-400 MHz	180-400 MHz
	SSB phase noise @ 5 MHz	L_{SSB}	-132 dBc/Hz[1]	-139 dBc/Hz[2]
PLL	reference frequency	f_{sys}	13,0 MHz	
	close to carrier phase noise	L_0	-84 dBc/Hz	
	charge pump current	I_{cp}	1,0 mA	
IF VGA	PN random wave input signal	$V_{\text{I/Q ac,max}}$		1100 $\text{mV}_{\text{pp,diff}}$
	input signal	$V_{\text{I/Q rms}}$		260 $\text{mV}_{\text{pp,diff}}$
	input resistance	$R_{\text{IF,diff}}$	1 kΩ	30 kΩ
	input capacitance	$C_{\text{IF,diff}}$	0.5 pF	1.0 pF
cascaded	voltage gain from VGA input to IQ output	$G_{\text{IQ,min}}$	-35 dB	
		$G_{\text{IQ,max}}$	70 dB	
	3rd-order input intercept point (source impedance 50Ω)	$\text{IIP3}_{\text{max gain}}$	-2 dBm	
		$\text{IIP3}_{\text{min gain}}$	-46 dBm	
	noise figure 1kΩ source resistance	$F_{\text{IQ,min}}$	7.0 dB	
		$F_{\text{IQ,max}}$	75 dB	
	carrier suppression	a_C		48 dB[3]
	single-sideband suppression	a_{SSB}		49 dB[3]
	3rd harmonic suppression @ $3f_{\text{IF}} - f_m$	a_{H3}		20 dB[1]
	dynamic range		98 dB	70 dB
	output voltage/level		1.0 $\text{V}_{\text{pp,diff}}$	-7.5 dBm
	3rd-order intermodulation	a_{IM3}		50 dB[1]
	adjacent channel leakage ratio	ACLR		-53 dBc[1]
	error vector magnitude	EVM	6.2 %	2.7 %
	output noise floor	$P_{\text{N, max gain}}$		-129 dBc/Hz[4]
	output noise floor	$P_{\text{N, min gain}}$		-160 dBm/Hz[4]
	I/Q amplitude mismatch	$\Delta V_{(\text{IQ})}$	1.5 dB	
	I/Q phase deviation	$\Delta\Phi_{(\text{IQ})}$	± 2.5 deg	
baseband filter	pass band	f_{bb}	1.92 MHz	1.92 MHz
current consumption	standby	I_{standby}	$<10\,\mu$A	$<10\,\mu$A
	synthesizer on	I_{synth}	11.0 mA	11.0 mA
	synthesizer + 1 channel	I_{ch1}	26.9 mA	30.4 mA[3]
	synthesizer + 2 channels	$I_{\text{ch1,2}}$	35.9 mA	
	ext. LO + 1 channel	I_{ch1}	14.5 mA	45.8 mA[3]
	ext. LO + 2 channels	$I_{\text{ch1,2}}$	23.6 mA	
	[1] @ 318 MHz	[2] @ 285 MHz		
	[3] @ $P_{\text{out}} = -12$dBm	[4] @ 20 MHz offset		